PGY-UHS II SD/SDIO UHS II Protocol Analyzer

PGY-UHS II SD/SDIO UHS II Protocol Analyzer is the most feature rich comprehensive Protocol Analyzer available to capture and debug UHS-II protocol data. PGY-UHS-II Protocol Analyzer supports FD156 and HD312 data rate. The innovative active probe has minimum electrical loading on device under test (DUT) and captures protocol data without affecting the performance of DUT. PGY-UHS II protocol analyzer allows streaming of protocol data from PGY-UHS II Protocol Analyzer to host system (using USB3.0 or GbE interface). Comprehensive decoding of data, protocol tests, and error analysis enables verification of communication between UHS II host and device.

PGY-UHS II Protocol Analyzer allows Design and Test Engineers to test and debug SD UHS-II Interface triggering on command, response, data or CRC errors. PGY-UHS II Protocol analyzer instantaneously provides decoding of CCMD, DCMD, MSG, DATA and its arguments. The Analytics feature offer graphical representation of command, response, and data and frequency of operation for the acquired duration.

Key features and benefits:

- Continuous monitoring and streaming of protocol data to capture elusive events (more than 30GB data capture)
- Protocol tests of captured data for protocol integrity, DCMD, CCMD, MSG and DATA
- Instantaneous display Protocol activity while he PGY-UHS II is capturing the Protocol data allowing almost live analysis of protocol activity
- Hardware based protocol aware trigger capability enables capturing specific events
- Trigger on CRC error conditions allow capturing infrequent error events
- User can identify the anomalies by decoding command and response argument
- Analytics provides analysis of acquired protocol data by plotting command, response, data and frequency of operation over acquired time
- Decoding of device registers for easy analysis
- Filter feature allows you to view specific packets in decoded protocol packets
- Search for specific events in protocol activity
- Easy to use software user interfaces reduces the learning curve of protocol analysis
- Software is designed to handle long duration capture and display the decoded data without demanding extensive resources in host computer
- Insertion of markers in protocol activity helps in correlating the input digital signal with Protocol Activity
- Trigger out signal for any specific protocol event allows triggering of other instruments such as oscilloscope
- Interface to host system using USB3.0 or Gigabit Ethernet interface
- Flexibility to upgrade the hardware firmware using GbE interface provides easy field up gradation of firmware
- Decoded data packets can be exported to CSV file for further analysis

Prodigy TECHNOVATIONS

PGY-UHS II SD/SDIO UHS II Datasheet

Specifications:

Interfaces Supported	:	SD4.0 (UHS-II), FD156 and HD312, SDIO
Protocol Decode	:	CCMD, DCMD, MSG, DATA, Arguments, Device registers
Data Decode	:	Supported
Protocol Test	:	Protocol Integrity, CRC Errors, Timing values, Data CRC Errors, Reserved commands
Storage Capability	:	Continuous streaming of protocol activity upto 30GB
Capture Mode	:	Manual Run/Stop, Time specific
Trigger on	:	DCMD, CCMD, MSG, SYN, BSYN, DIR, LIDL, DIDL, SDB, SOP, EOP, EDB
Trigger Actions	:	Capture data and/or trigger out signal
Host Machine Minimum Requirements	:	Microsoft Windows® 8, Windows 7, 16GB of RAM; Storage with at least 50 GB HDD space for the storing the acquired data display with resolution of at least 1024x768

Setup

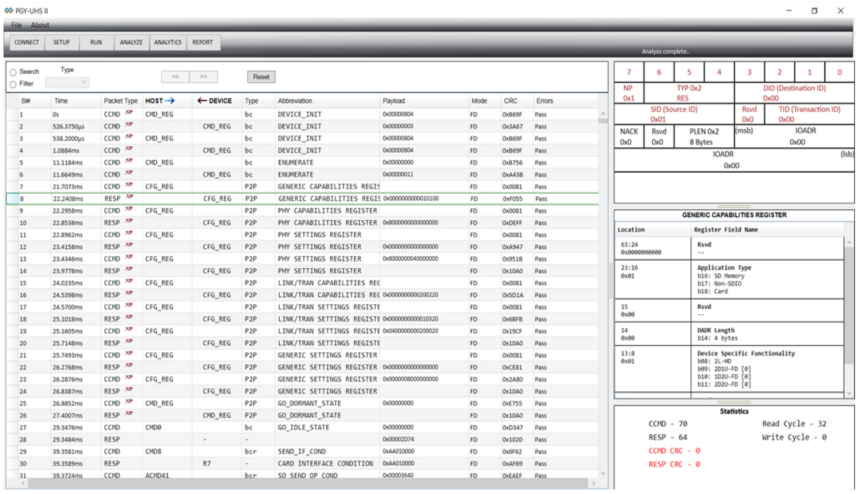
PGY-UHS II Protocol Analyzer provides USB3.0 and GBe interface for host connectivity. PGY-UHS II software runs in host machine enables configuration of PGY-UHS II hardware for UHS II protocol analysis storage

UHS II Interposers:

Prodigy Technovations provides UHS II fixture /interposer. This allows user to probe UHS II Signals to monitor the protocol between host and device.

Comprehensive Protocol Analysis

PGY–UHS II Software provides industry best protocol analysis capabilities. Easy to use interface reduces the protocol analysis time. Time stamped view of protocol decode listing provides easy view of protocol activities between host and device. At click of a button user can get decode of argument of Response from the device. Decoding of registers provides detail information on devices. Analytics features quickly provide insight into protocol activity without going through the complete protocol activity.



Powerful Decide capabilities Registers

PGY-UHS II Protocol Analyzer quickly decodes the UHS II register and displays register filter name. These decode tables allow identify the host and device setting being set and quickly debug it. Above image displays the Generic capabilities and settings between host and device.

7	6	5	4	3	2	1	0
NP 0x0	TYP 0x2 RES			DID (Destination ID) 0x00			
SID (Source ID) 0x01				Rsvd 0x00	TID (Transaction ID) 0x00		
NACK 0x0	Rsvd 0x00						
Rsvd 0x0	APP 0x0	CMD_INDEX 0x03					
SD_Arg 0x20050100							

Payload Details

New Published RCA of the card[31:16] = 0010000000000101b
Card status bits[15:0] = 0000000100000000b
Bit [15] = 0b;COM_CRC_ERROR(no error)
Bit [14] = 0b;ILLEGAL_COMMAND(no error)
Bit [13] = 0b;CARD_ECC_FAILED(no error)
Bit [9,10,11,12] = 0000bCURRENT_STATE(Idle)
Bit [8] = 1b;READY_FOR_DATA(Ready)
Bit [7] = 0b;Reserved
Bit [6] = 0b;FX_EVENT(No event)
Bit [5] = 0b;APP_CMD(Disable)
Bit [4] = 0b;Reserved for SD I/O card
Bit [3] = 0b;AKE_SEQ_ERROR(no error)
Bit [2] = 0b;Reserved_Appln_Specific commands
Bit [1] = 0b;Reserved_For_Manufacturer
Bit [0] = 0b;Reserved_For_Manufacturer

Decoding of Payload bits

7	6	5	4	3	2	1	0
NP 0x1	TYP 0x0 CCMD			DID (Destination ID) 0x00			
SID (Source ID) 0x00				Rsvd 0x0	TID (Transaction ID) 0x00		
R/W 0x1	Rsvd 0x0	PLEN 0x1 4 Bytes		(msb) IOADR 0x02			
IOADR 0x02							(lsb)
Payload							

DEVICE_INIT

Property	Description
Group Descriptor	0x00
Group Allocated Power	1440 [mW]
Device Allocated Powe	360 [mW]
Completion Flag	All Devices Complete Initialization

Decoding of Device Init

7	6	5	4	3	2	1	0
NP 0x1	TYP 0x2 RES			DID (Destination ID) 0x00			
SID (Source ID) 0x01				Rsvd 0x0	TID (Transaction ID) 0x00		
NACK 0x0	Rsvd 0x0	PLEN 0x2 8 Bytes		(msb) IOADR 0x00			
IOADR 0x00							(lsb)

GENERIC CAPABILITIES REGISTER

Location	Register Field Name
63:24 0x000000000	Rsvd --
23:16 0x01	Application Type b16: SD Memory b17: Non-SDIO b18: Card
15 0x00	Rsvd --
14 0x00	DADR Length b14: 4 bytes
13:8 0x01	Device Specific Functionality b08: 2L-HD b09: 2D1U-FD [0] b10: 1D2U-FD [0] b11: 2D2U-FD [0]

Generic Capabilities Register Decode

7	6	5	4	3	2	1	0
NP 0x1	TYP 0x0 CCMD			DID (Destination ID) 0x01			
SID (Source ID) 0x00				Rsvd 0x0	TID (Transaction ID) 0x00		
R/W 0x1	Rsvd 0x0	PLEN 0x2 8 Bytes		(msb) IOADR 0x00			
IOADR 0x08							(lsb)
Payload							

GENERIC SETTINGS REGISTER

Location	Register Field Name
63 0x01	Rsvd b63: DLSM transits to Active state
62:32 0x00000000	Rsvd --
31:12 0x000000	Rsvd --
11:8 0x00	Number of Lanes and Functionality 2 Lanes FD/2L-HD mode
7:1 0x00	Rsvd --
0 0x00	Power Control Mode b0: Fast Mode

Generic Setting Register Decode

PGY-UHS II SD/SDIO UHS II Datasheet

7	6	5	4	3	2	1	0
NP 0x1	TYP 0x0 CCMD			DID (Destination ID) 0x01			
SID (Source ID) 0x00				Rsvd 0x0	TID (Transaction ID) 0x00		
R/W 0x1	Rsvd 0x0	PLEN 0x2 8 Bytes		(msb) IOADR 0x00			
IOADR 0x0C							(lsb)
Payload							

7	6	5	4	3	2	1	0
NP 0x1	TYP 0x2 RES			DID (Destination ID) 0x00			
SID (Source ID) 0x01				Rsvd 0x0	TID (Transaction ID) 0x00		
NACK 0x0	Rsvd 0x0	PLEN 0x2 8 Bytes		(msb) IOADR 0x00			
IOADR 0x02							(lsb)

LINK/TRAN SETTINGS REGISTER

Location	Register Field Name
63:40 0x000000	Rsvd --
39:32 0x04	N_DATA_GAP Min DIDL: 4
31:20 0x0200	MAX_BLKLEN Max Payload length: 512
19:18 0x00	Rsvd --
17:16 0x00	MAX_RETRY_NUM DATA burst retry disabled
15:8 0x20	N_FCU Max Block Number in FCU: 32
7:0 0x00	Rsvd --

PHY CAPABILITIES REGISTER

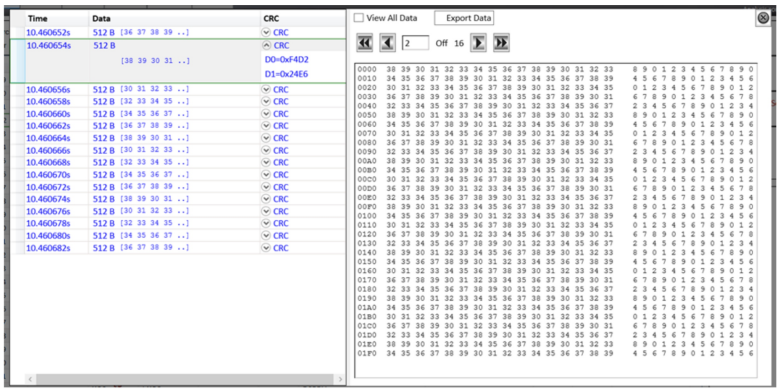
Location	Register Field Name
63:40 0x000000	Rsvd --
39:36 0x08	Device-Specific N_LSS_DIR DIR LSS: 64
35:32 0x00	Device-Specific N_LSS_SYN SYN LSS: 64
31:16 0x0000	Rsvd --
15 0x00	Supporting Hibernate Mode b15: No Hibernate Mode
14:6 0x0000	Rsvd --
5:4 0x00	PHY Major Revision UHS156

LINK/TRAN Setting Register Decode

PHY Capabilities Register Decode

Data Packet Analysis:

PGY-UHS II automatically identified if data transfer is FD156 and HD512 mode. PGY-UHS II will decode data commands and identifies, if data is in HD and FD mode and captures data. Display of captures can be viewed for each command. Data block is displayed as below



Software will validates CRC values and highlights in red color, for any CRC failure. Data is displayed iin HEX and ASCII format for each block.

Analytics:

PGY-UHS II offers analytical feature displays time stamped packets of host, device and data exchange in a time domain view. This allows user to look at protocol activity traffic between the host and device.

User can export the Protocol decoded to txt file for documentation and further analysis in a user environment.

Ordering information:

PGY- UHS II UHS II SD/SDIO Protocol Analyzer

(Shipment includes Hardware, software CD, one set probe, USB3.0 and Ethernet Cable, Power Adopters, UHS II interposer)

Warranty:

Hardware and software carries warranty of one year.

Probes are covered three months warranty for any manufacturing defects

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