

# PGY-UFS 4.0-PA MPHY, UniPro, UFS Protocol Analzyer



PGY-UFS 4.0-PA, UFS Protocol Analyzer is the industry first working and tested UFS 4.0 Protocol Analyzer. It offers protocol data capture and debug of data across MPHY, UniPro and UFS protocol layers. It allows for instantaneous decoding of UFS, UniPro and MPHY layers with flexibility to correlate decoded data across these protocol layers. PGY-UFS 4.0-PA supports PWMG1 to HSG5B data rates and two TX, two RX lane decode. The active probe has minimum electrical loading on device under test (DUT) and captures protocol data without affecting the performance of DUT. PGY-UFS 4.0-PA Protocol Analyzer support two lane data. Comprehensive on the fly decoding of UniPro & UFS data enables validation of communication between UFS host and device.

PGY-UFS 4.0-PA Protocol Analyzer allows Design and Test Engineers to obtain deep insight into UFS host and device communication. MPHY/UniPRO/UFS packet-based triggering allows specific protocol data capture and analysis. PGY-UFS Protocol analyzer instantaneously provides decoding of UFS, UniPro and MPHY layers with a correlation to MPHY, UniPro and UFS layers.

Solder down active probes allows probing the MPHY test points. This allows the design and test engineers to capture UFS traffic between the host and UFS memory with high signal fidelity. Today's test engineers need to test the use case scenarios in their labs that mimic real-life use cases. The PGY-UFS 4.0-PA, UFS Protocol Analyzer has been designed to enable engineers to closely monitor and analyze the traffic between the host and the device while executing the various use case scenarios.

nect	Acquire Sto	p Acq Stop Trans	sfer Stop Reset	Time Δt1 M0	M1	= 170.2375ms	Δt2 M0 ~	M1	= 170.2375ms	UFS, Time		P0 ~	P1	= 348.5	5025ms Δt2	PO	v P1	~  =	
View	DeviceCon	figView Analy	tics View PacpVi	ew Report View T	riggerVi	ew Color Se	ettings						=	SymbolsV	iew_HOST	Search	/iew		
	Index	Timestamp	Host	Device	Gear	Task Tag	Total EHS Len	gth	Segment Length	Data Offs	et LUN	Status		Index	K\D Code	8 Bit	Lane	Gear	
	8	531.9985ms		RESPONSE	HS_G5B	03	00		0000		01	Good		862	D3.1		Tx	HS_G5B	
	9	648.9097ms	WRITE_10		HS_G5B	04	00		0000		01			863	D3.1	0x23 0x23	Tx	HS_G5B	
	10	673.8643ms		READY_TO_TRANSFER	HS_G5B	04	00		0000		01			864	D3.1	0x23	Tx	HS_G5B HS_G5B	
	11	702.2748ms	DATA OUT		HS_G5B	04	00	$\rightarrow$	1000	00000000	01			866	D3.1	0x23	Tx	HS_G5B	
	12	702.2782ms	_	RESPONSE	HS_G5B	04	00		0000		01	Good		867	D3.1	0x23	Tx	HS_G5B	
	13	777.6731ms	READ 10		HS G5B	05	00		0000		01			868	D3.1	0x23	Tx	HS_G5B	
	14	827.1691ms		DATA IN	HS_G5B	05	00		1000	00000000	01			869	D3.1	0x23 0x23	Tx	HS_G5B HS_G5B	
				_						00000000		C4		870	D3.1	0x23	Tx	HS_G5B	
	15	827.1709ms		RESPONSE	HS_G5B	05	00		0000		01	Good		872	D3.1	0x23	Tx	HS_G5B	
	16	944.0402ms	WRITE_10		HS_G5B	06	00		0000		01			873	D3.1	0x23	Tx	HS_G5B	
	17	968.9898ms		READY_TO_TRANSFER	HS_G5B	06	00		0000	15	01			874	K28.5	0xBC	Tx	HS_G5B	
	18	997.4088ms	DATA_OUT		HS_G5B	06	00		1000	00000000	01			875	D7.1 D5.1	0x27 0x25	Tx	HS_G5B HS_G5B	
	19	997.4122ms		RESPONSE	HS_G5B	06	00		0000		01	Good		877	D30.4	0x25 0x9E	Tx	HS_G5B	
	20	1.072827s	READ 10		HS G5B	07	00		0000		01		-	878	K28.5	0xBC	Tx	HS G5B	
ProV	Index	Timestamp	Host	Device	Gear	DestDeviceID	DestCPortID	EOM	Frame Seq Cre	dit Value	CRC		Т	Index	iew_DEVICE	8 Bit	Lane	Gear	
	1381	997.4094ms	DL_DATA		HS_G5B	01	00	00	09					3028	D0.0	0x00	Rx	HS_G5B	
	1382	997.4094ms		DL_AFC	HS_G5B				07 9B					3029	D0.0	0x00	Rx	HS_G5B	
	1383	997.4096ms		DL_AFC	HS_G5B				08 A4				-1	3030	D0.0	0x00	Rx	HS_G5B	
	1384	997.4096ms	DL_DATA		HS_G5B	01	0.0	00	ØA .					3031 3032	D0.0	0x00	Rx Rx	HS_G5B HS_G5B	
	1385	997.4098ms		DL_AFC	HS_G5B				09 AC					3033	D0.0	0x00	Rx	HS_G5B	
	1386	997.4099ms	DL DATA		HS G5B	01	80	00						3034	K28.5	0xBC	Rx	HS_G5B	
	1387	997.41ms	DC_DATE	DL_AFC	HS_G5B	01	00	00	ØA B5				_	3035	D7.1	0x27	Rx	HS_G5B	
			DI DITA	DL_APC		0.0		0.0						3036	D5.3	0x65	Rx	HS_G5B	
	1388	997.4101ms	DL_DATA		HS_G5B	ØI.	90	00						3037 3038	D26.3 K28.5	0x7A 0xBC	Rx Rx	HS_G5B HS_G5B	
	1389	997.4102ms		DL_AFC	HS_G5B				ØB BD					3039	D3.6	0xC3	Rx	HS_G5B	
	1390	997.4103ms	DL_DATA		HS_G5B	01	00	00	ØD O					3040	D23.1	0x37	Rx	HS_G5B	
	1391	997.4105ms		DL_AFC	HS_G5B				0C C6					3041	D18.4	0x92	Rx	HS_G5B	
	1392	997.4105ms	DL_DATA		HS_G5B	01	00	00	ØE					3042 3043	D5.5 D1.7	0xA5 0xE1	Rx	HS_G5B HS_G5B	
	1393	997.4107ms		DL AFC	HS G5B				ØD CE			_		3043	D1./	0xE1	Rx	HS_G5B	



Windows based protocol analysis software provides industry best protocol correlation between UFS to UniPro and MPHY layers. Time correlation between the different protocol layers significantly reduces debug time of designs. Floating window design of this software allows engineers to view UFS view, UniPro view and MPHY view on different computer monitors and automatically correlate the UFS packets to MPHY layer. This makes analysis very easy while analyzing the gigabytes of Protocol information.

#### **Key Features**

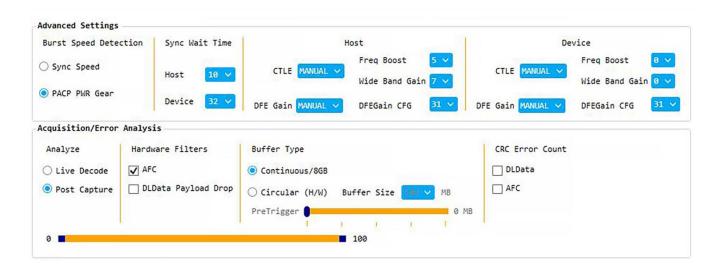
- ♦ Supports version MPHY 4.0, UniPro 1.8 and UFS v2.1/3.1/4.0
- Supports PWM G1 to G7 and HS G1,2,3, 4, 5 Rate A and B Series
- ♦ Supports one/two data lanes (2 TX and 2 RX)
- Flexibility to capture very large data using continuous streaming of Protocol data to host computer
- with 16GB Internal acquisition memory field upgradable up to 64GB
- ♦ Hardware based resizable circular buffer with pre/post trigger
- ♦ Flexibility to decode selected data from 16GB buffer
- ♦ Solder down active probe provide high signal fidelity
- ♦ Decoding at MPHY, UniPro and UFS layers
- Trigger based on MPHY, UniPro and UFS layers packet content
- Trigger out signal at trigger event allows the triggering of other instruments such as oscilloscope
- ♦ Interface to host system using USB 3.0
- Flexibility to upgrade the hardware firmware using GbE interface provides easy field upgradation of FPGA firmware
- ♦ Decoded data packets can be exported to txt file for further analysis
- Light weight and can be deployed for on-site/ field tests



### **Test Setup**

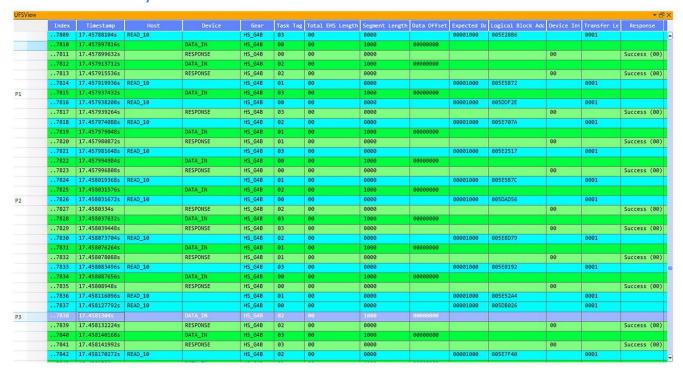


PGY-UFS 4.0-PA UFS Protocol Analyzer interfaces to solder down probe tips using mSMP flexi coax cables. The active probe tips are powered by power module which is powered by PGY-UFS4.0-PA. Protocol Analyzer is interfaced to host computer using USB3.0 interface. High-speed host connectivity and 16GB buffer enables continuous streaming of protocol data to host SSD and storage for longer period of time. Software offers multi-view such as MPHY view, UniPro view and UFS View. Each view lists the respective protocol packets and its details with correlation of each layer for easy debug. Lightweight Analyzer is easy to carry during field visit.



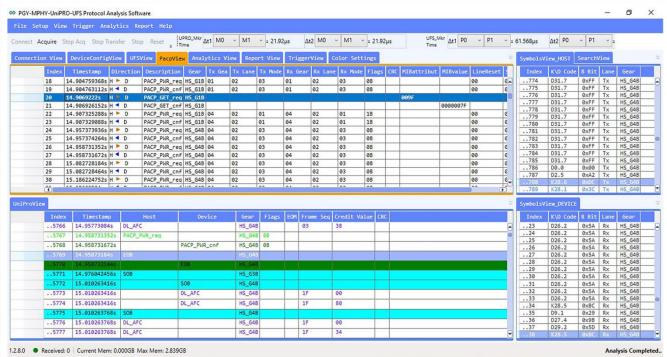


#### **UFS Protocol Layer**



PGY-UFS 4.0-PA Software can display each UFS packet parameters in a listing window. Right click lists all the packet parameter for user selection. User can color code the fonts or background color for easy identification for each UFS packet.

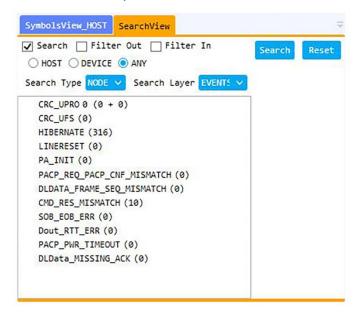
## PACP And Unipro View



PGY-UFS 4.0-PA Software separates the PACP packets in a separate view for easy analysis of power mode change packets and link to UniPro packets. Users can view the MPHY states stall, prepare, sync information in UniPro view apart from user selection for DL\_Data and AFC/NACK Packet details.



#### Error Events, Search and Filter



PGY-UFS 4.0-PA Software does the live decode and list all the events. The list of events are shown in this picture. Users can easily note the errors in captured protocol data. In large buffer capture, it takes extremely difficult to locate the errors. But PGY-UFS4.0-PA software simplifies this by listing events while decoding the captured data. Search and Fliter allows you directly locate the error events or UFS or UniPro or PACP packet in the protocol listing windows. Filter-in and Filter-out makes it easy view the data of interest in the protocol listing window.

## Comprehensive Protocol Analysis Using Multi-View



PGY-UFS 4.0-PA UFS Protocol Analyzer provides USB 3.0 interface for host computer connectivity. High-speed host connectivity enables continuous streaming of protocol data to host HDD and storage for long period of time. Software offers multi-view such as MPHY view, UniPro view and UFS View. Each view lists the respective protocol packets and its details with correlation of each layer for easy debug.

PGY Protocol Analyzer's easy to use interface, reduces the protocol analysis time. Time stamped view of protocol decode listing provides easy view of protocol activities between host and the device. At a click of a button, user can view the decode of each packet and the intended function. Floating window software architecture allows the user to view each protocol layer on separate monitors for easy debug. Autocorrelation of each selected packet from UFS to MPHY layers simplifies the debug activity



# Specifications

Data Rates Supported	PWM G1 to G7, High Speed Gear 1, Gear 2, Gear 3, Gear 4, Gear 5 and Rate A and B					
Link width	Configurable for 1TX/1RX or 2TX/2RX					
Probes	Solder Down Active Probes					
Protocol Decode	MPHY, UniPro and UFS layers					
Trace Capture Size	Supports Continuous streaming of Protocol data to Host computer SSD/HDD. Internal acquisition memory 16GB expandable up to 64GB					
Trigger	Based MPHY, UniPro, UFS Packets					
Front Panel Connectors	Interface for Active probes. Trigger in/out SMA connectors					
Interface for Host Computer	USB 3.0 and Gigabit Ethernet interface					
Host Computer Requirements	Windows 7/8.0/8.1/10 64bit operating System with i7/i9 intel processor. System RAM of minimum 16GB, the product would give a faster response for a 32GB. The minimum storage capacity of 100GB should be available in the hard disk drive. User can use more storage based on trace storage requirement.  Display resolution of the monitor is 1024X768. Host computer should support USB3.0 interface.					
Dimension	(W x H x D) (20.5X5X25) cms					
Weight	Approx. 2.5Kg					
Power Requirement	12V, 3A DC Power Supply (AC/DC Supplied along with Analyzer)					



# **Trigger Specifications**

Stack	Protocol Analyzer	Packet Type						
		(TRG_UPRO0)						
	Link Start-up Sequence	(TRG_UPRO1)						
		(TRG_UPRO2)						
		PACP_PWR_reg						
		PACP_PWR_cnf						
		PAC_Cap_ind						
		PACP_Cap_EXT1_ind						
		PACO_EPR_ind						
		PACP_TestMode_req						
UniPRO	PHY Capability Adapter	PACP_GET_req						
Ollipko	Packets (PACP)	PACP_GET_cnf						
		PACP_SER_req						
		PACP_SET_cnf						
		PACP_TEST_Data_0						
		PACP_TEST_Data_1						
		PACP_TEST_Data_2						
		PACP_TEST_Data_3						
		SOF						
		EOF						
		EOF_ODD						
	Data Link Packets	EOF_EVEN						
		COF						
		AFC/NAC						
		Traffic class 0/Traffic class 1						
		NOP IN						
		NOP OUT						
		Commands						
UFS	UFS Layers Packets	Response						
	2.3.24,0.0.000	Task Management Request						
		Task Management Response						
		Ready To Transfer						
		Ready to Transfer						



## Solder Down Probe Tips for UFS3.0 and 3.1







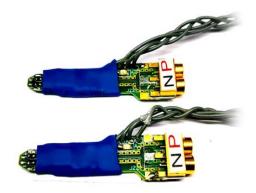
P5021-L-WE 14 Gbps probe tips with passive equivalizer at input

P5021-L 14 Gbps probe tip with isolation resistor

P5021 14 Gbps probe tips for direct access to test points

Probing UFS signal is one of the key challenges in reliable UFS protocol decode. In most of the DUT, test points are located close to each other without enough space to solder the probe tips. Prodigy Technovations offers three type of 14 Gbps Probe tips which provides flexibility to choose the probe tips to meet the need. P5021-L and P5021-L-WE Probe tips has isolation resistor which can be changed based signal strength at test points. This helps in reducing reflections while accessing the test point and maintaining the signal integrity. The passive equalizer in P5021-L-WE helps in maintaining the differential impedance between the lanes. If test points are easily accessible, then P5021 probe tip can be used to probe the test points.

## Solder Down Probe Tips for UFS 4.0



Prodigy Technovations provides innovative solder down active probe tips, which can equalize the MPHY signals upto MPHY HSG5B speed and amplify the signal to support cable loss in mSMP cable and PCB trace in analyzer. These probe tips are tested with real world UFS4.0 host/device test and development platform.

If you need probe card/tips with mSMP connector to mate with device under test mSMP connector, please contact Prodigy Technovations at contact@prodigytechno.com



### **Ordering Information**

PGY-UFS 4.0-PA UFS 4.0 Protocol Analyzer

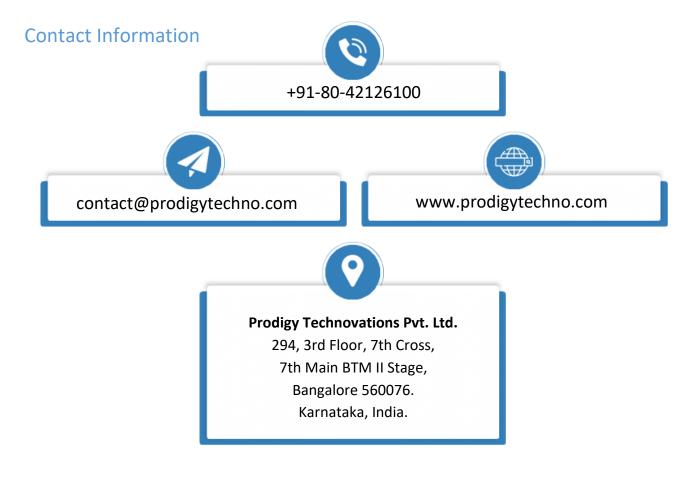
(Shipment includes Hardware, software CD, One set probe, USB 3.0, Ethernet Cable and Power adapter)

Note: Supports UFS2.0/2.1/3.0/3.1

## Warranty Information

Hardware and software carries a warranty of 1 year.

Probes are covered for a 3 month warranty for any manufacturing defects



## **About Prodigy Technovations Pvt Ltd.**

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical Layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.